Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A failure analysis system having software incorporated therein, comprising:

a function to record a test terminal signal information of a testing logic LSI as a target of analysis in synchronization with a clock signal;

a function to reproduce said test recorded terminal signal information in synchronization with the clock signal; and

a function to compare said reproduced terminal signal information with a reference terminal signal information of a normal logic LSI[[; and]],

wherein the test terminal signal information includes a trace data map of a condition change in a register data and a RAM data for a specific period of time.

Claim 2-6 (Canceled)

Claim 7 (Currently Amended): A failure analysis system according to claim 1 [[2]], wherein said failure analysis system further has a function to generate a plurality of trace difference maps by generating a plurality of defects and to obtain an average and

a data spread of a difference by a statistical work.

Claim 8 (Canceled)

Claim 9 (Previously Presented): A failure analysis system according to claim 1, wherein said failure analysis system further has a function to record a command trace data of a CPU in synchronization with said reference terminal signal information.

Claim 10 (Canceled)

Claim 11 (Previously Presented): A failure analysis system according to claim 1, wherein said failure analysis system further has a function to connect comparative signals of a plurality of logic LSIs to multiinput OR terminals and to analyze a plurality of logic LSIs at the same time.

Claim 12 (Previously Presented): A failure analysis system according to claim 1, wherein said test terminal signal information also includes an analog signal information.

Claim 13 (Previously Presented): A failure analysis system according to claim 12, wherein said failure analysis system further has a function to obtain in advance analog/digital difference properties of the testing logic LSI and the normal logic LSI, or

digital/analog difference properties thereof and to correct an analog conversion property.

Claim 14 (Previously Presented): A failure analysis system according to claim 12, wherein said testing logic LSI has an on-chip debugger mounted thereon.

Claim 15 (Previously Presented): A failure analysis system according to claim 1, wherein said failure analysis system further has layered software.

Claim 16 (Previously Presented): A failure analysis system according to claim 1, wherein the target of analysis is a system having a logic LSI mounted thereon.

Claim 17 (Currently Amended): A failure analysis method comprising:

recording a test terminal signal information of a testing logic LSI as a target of analysis in synchronization with a clock signal;

reproducing the recorded test terminal signal information in synchronization with the clock signal; and

comparing the reproduced test terminal signal information with a reference terminal signal information of a normal logic LSI[[; and]],

wherein the test terminal signal information includes ~~producing~~ a trace data map of a condition change in a register data and a RAM data for a specific period of time.

Claims 18-22 (Canceled)

Claim 23 (Currently Amended): A failure analysis method according to claim [[18]] 17, further comprising:

generating a plurality of trace difference maps by generating a plurality of defects; and

obtaining an average and a data spread of a difference by a statistical work.

Claim 24 (Canceled)

Claim 25 (Previously Presented): A failure analysis method according to claim 17, further comprising recording a command trace data of a CPU in synchronization with the reference terminal signal information.

Claim 26 (Canceled)

Claim 27 (Currently Amended): A failure analysis method according to claim 17, further comprising:

connecting a plurality of comparative signals of a plurality of logic LSIs to a plurality of multiinput OR terminals; and

analyzing the plurality of logic LSIs at the same time.

Claim 28 (Previously Presented): A failure analysis method according to claim 17, wherein the test terminal signal information also includes an analog signal information.

Claim 29 (Previously Presented): A failure analysis method according to claim 28, further comprising:

obtaining in advance analog/digital difference properties of the testing logic LSI and the normal logic LSI, or digital/analog difference properties thereof; and

correcting an analog conversion property.

Claim 30 (Previously Presented): A failure analysis method according to claim 28, wherein the testing logic LSI has an on-chip debugger mounted thereon.

Claim 31 (Previously Presented): A failure analysis method according to claim 17, wherein the target of analysis is a system having a logic LSI mounted thereon.